

FIG. 1
(Prior Art)

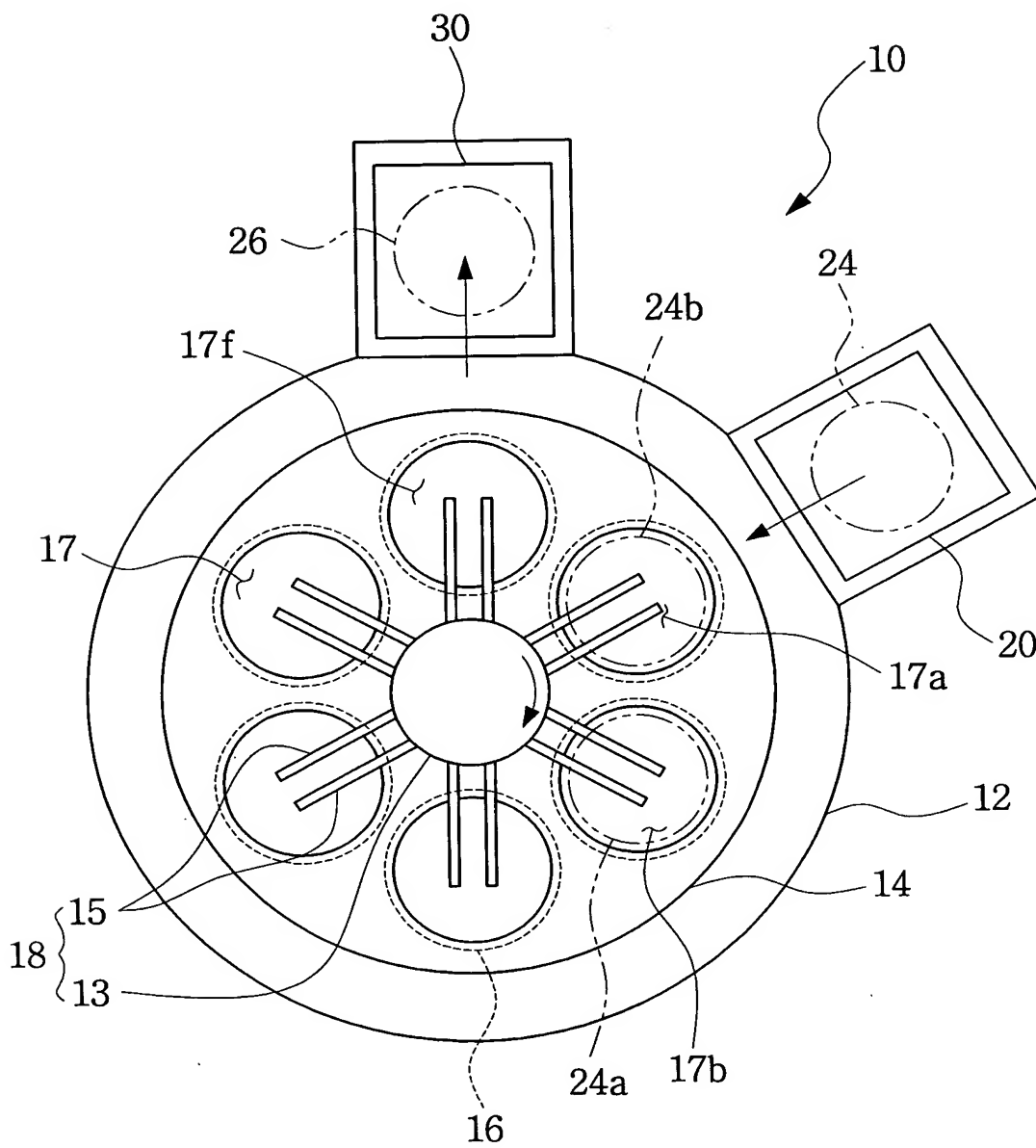


FIG. 2
(Prior Art)

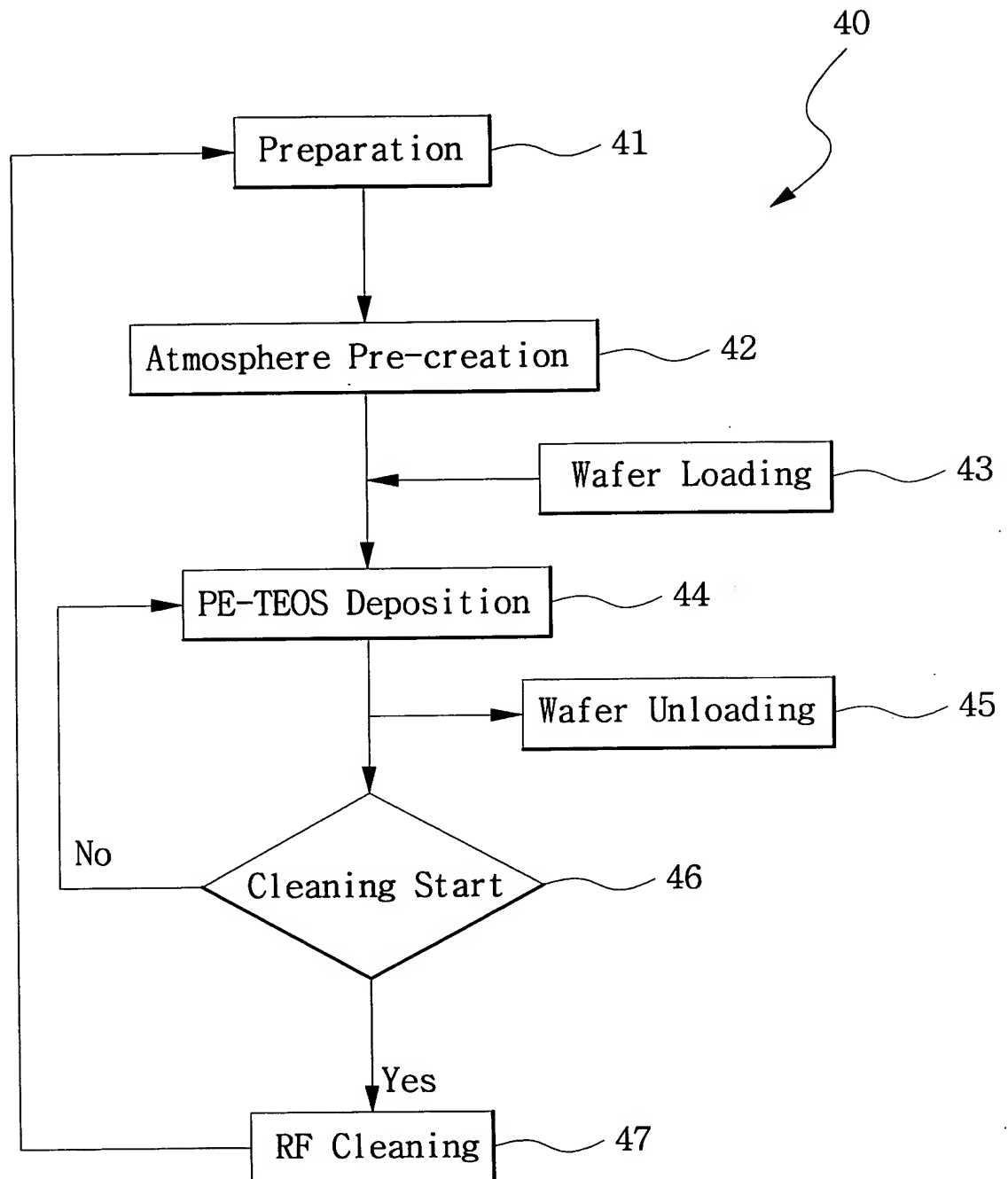


FIG. 3
(Prior Art)

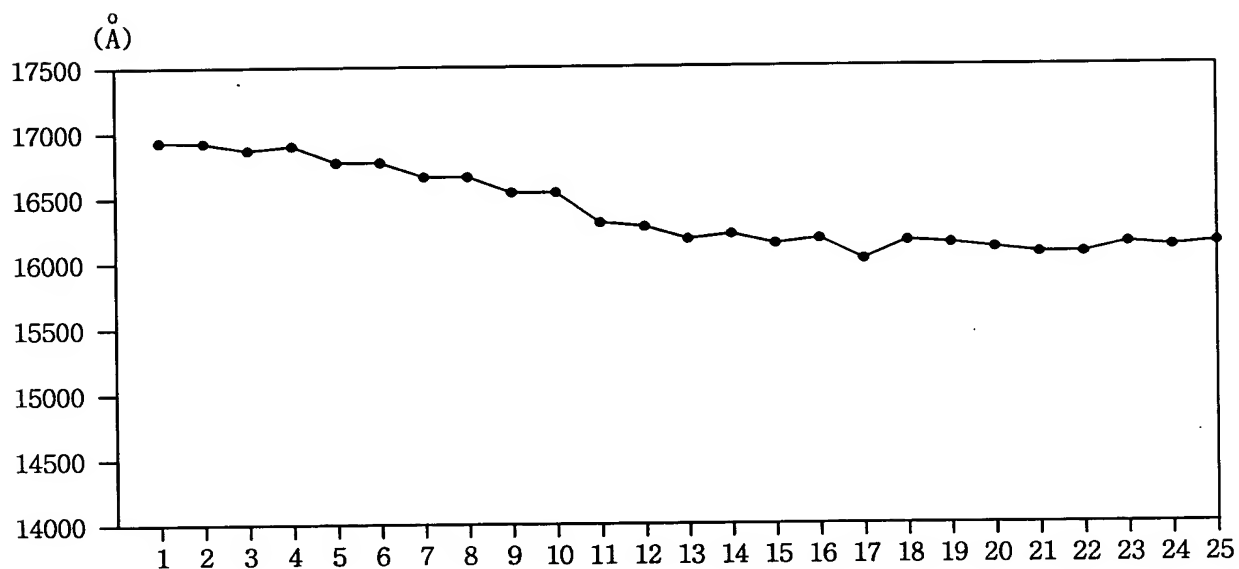
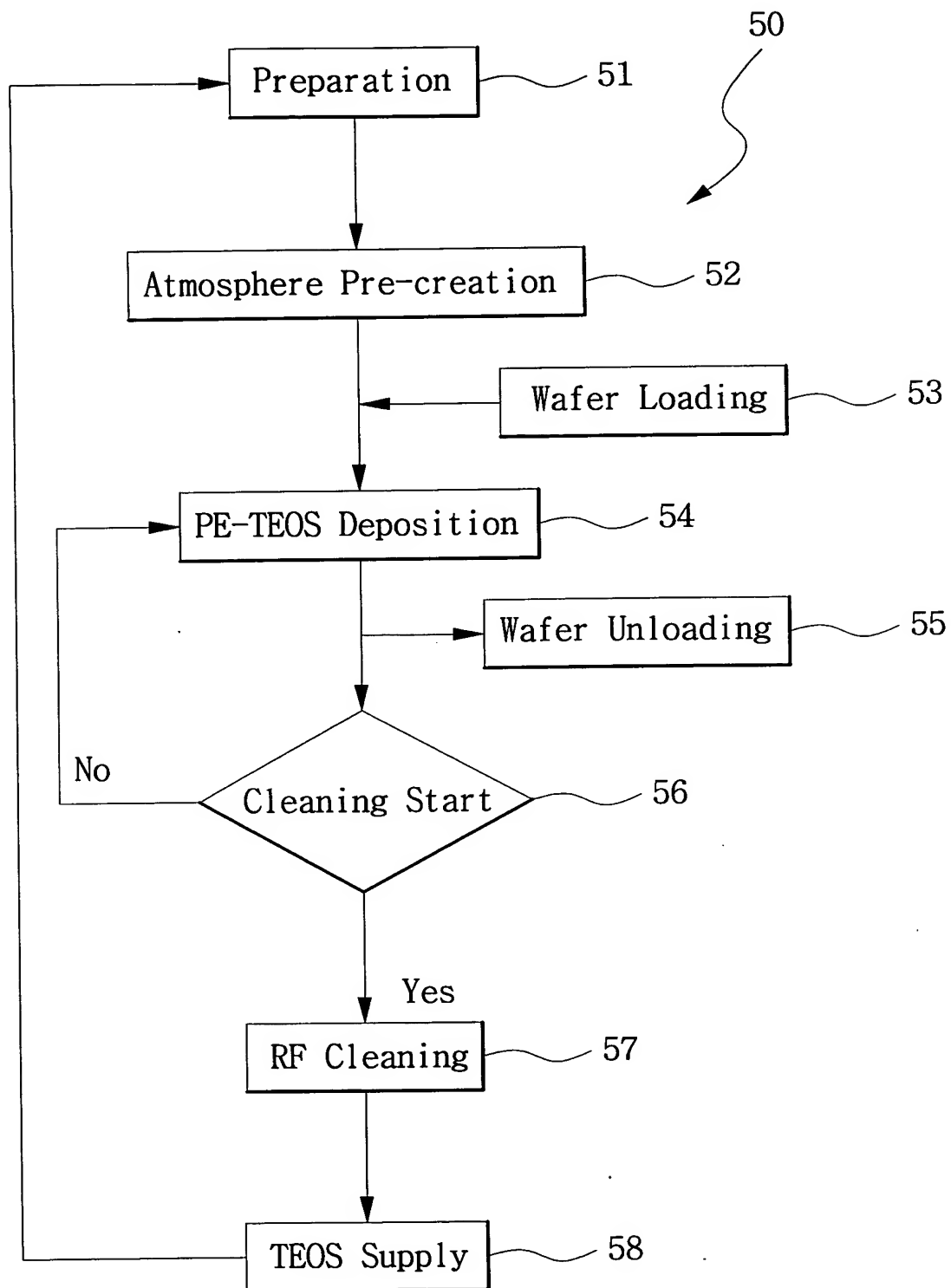


FIG. 4



METHOD FOR FORMING PE-TEOS LAYER OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

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FIG. 5

